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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,054	07/06/2001	Yi-Chuan Ding	JCLA6831	7810

7590 06/28/2002

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/900,054	DING ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. Claim 1 is objected to because of the following informalities: In claim 1, line 11, after "wafer," insert "wherein". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egawa et al. (U.S. Patent 6,376,278) in view of Belke, Jr. et al. (U.S. Patent 6,326,241) and Hung (U.S. Patent 6,380,624).

Egawa teaches a flip chip packaging process comprising (See col. 7, line 2 to col. 8, line 9 and FIGS. 7-9(A)):

providing a wafer 10 having a plurality of chips 18 formed thereon, wherein each chip has an active surface 10a;

providing a plurality of substrates 42, wherein each substrate includes at least a package unit;

respectively mounting the substrates onto the wafer such that each package unit corresponds to each chip wherein two neighboring substrates are separated by a gap 68;

filling an underfill material 34 between the substrates and the wafer, wherein the underfill material being introduced through the gaps between the substrates and from the boundary of the wafer;

solidifying the underfill material; and

dicing the wafer and the substrates to form a plurality of individualized packages 66, each individualized package including one chip and one package unit wherein the surface of each package unit is equal to the active surface of the corresponding chip.

Egawa fails to teach that each chip has an active surface provided with a plurality of bonding pads and each package unit having a plurality of contact pads wherein a gold bump is formed on each bonding pad and the contact pads are respectively connected to the corresponding bumps as recited in present claims 1 and 5.

Belke teaches a flip-chip12 has an active surface provided with a plurality of bonding pads 14 and a substrate having a plurality of bonding pads 20 wherein a gold bump 16 is formed on each bonding pad of the flip-chip and the bonding pads of the substrate are respectively connected to the corresponding bumps. See col. 4, line 58 to col. 5, line 12 and FIGS. 1-2. ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Belke's teaching into Egawa's method because doing so can provide the electrical inputs and outputs to the flip-chip 12. See col. 4, lines 63-66 and FIGS. 1-2.

Egawa fails to teach that each substrate includes a plurality of patterned conductive layers alternately laminated with a plurality of insulating layers wherein the

material of the insulating layer is FR-4, FR-5, bismaleimide triazine (BT), polymide, or materials composite of epoxy and ceramic as recited in present claims 2-4.

Hung teaches a substrate 228 includes a plurality of patterned copper films (236a and 236b) alternately laminated with a plurality of insulating layers 230 wherein the material of the insulating layer is FR-4, FR-5 and bismaleimide triazine (BT). See col. 4, lines 6-20 and FIG. 4. ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Hung's teaching into Egawa's method because doing so can make the production and the assembly of the memory module easier. See col. 1, lines 65-67.

3. Claims 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egawa et al. (U.S. Patent 6,376,278) in view of Belke, Jr. et al. (U.S. Patent 6,326,241) and Hung (U.S. Patent 6,380,624).

Egawa teaches a flip chip packaging process comprising (See col. 7, line 2 to col. 8, line 9 and FIGS. 7-9(A)):

providing a wafer 10 having a plurality of chips 18 formed thereon, wherein each chip has an active surface 10a;

providing a plurality of substrates 42, wherein each substrate includes at least a package unit;

respectively mounting the substrates onto the wafer such that each package unit corresponds to one chip wherein two neighboring substrates are separated by a gap 68;

filling an underfill material 34 between the substrates and the wafer, wherein the underfill material being introduced through the gaps between the substrates and from the boundary of the wafer;

solidifying the underfill material; and

dicing the wafer and the substrates to form a plurality of individualized packages 66, each individualized package including one package unit and one chip wherein the surface of each package unit is equal to the active surface of the corresponding chip.

Egawa fails to teach that each chip provided with a plurality of bonding pads and each package unit having a plurality of contact pads wherein a gold bump is formed on each contact pad and the bonding pads are respectively connected to the corresponding bumps as recited in present claims 7 and 11.

Belke teaches a flip-chip12' has an active surface provided with a plurality of contact pads 20' and a substrate 18' having a plurality of bonding pads 14' wherein a gold bump 16' is formed on each bonding pad of the substrate and the contact pads of the flip-chip are respectively connected to the corresponding bumps. See col. 4, lines 66-67 and col. 6, lines 30-48 and FIGS. 2-3. ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Belke's teaching into Egawa's method because doing so can provide the electrical inputs and outputs to the flip-chip 12. See col. 4, lines 63-66 and FIG. 3.

Egawa fails to teach that each substrate includes a plurality of patterned conductive layers alternately laminated with a plurality of insulating layers wherein the

material of the insulating layer is FR-4, FR-5, bismaleimide triazine (BT), polymide, or materials composite of epoxy and ceramic as recited in present claims 8-10.

Hung teaches a substrate 228 includes a plurality of patterned copper films (236a and 236b) alternately laminated with a plurality of insulating layers 230 wherein the material of the insulating layer is FR-4, FR-5 and bismaleimide triazine (BT). See col. 4, lines 6-20 and FIG. 4. ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Hung's teaching into Egawa's method because doing so can make the production and the assembly of the memory module easier. See col. 1, lines 65-67.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
June 26, 2002

LONG PHAM
PRIMARY EXAMINER